Refine Search

Search Results -

Terms	Documents
(compact same layout$1 same node$1 same edge$1) and (parent same descendent$1)	0

Database:
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Set Name side by side	Query	Hit Count	Set Name result set
	DB=PGPB; PLUR=YES; OP=ADJ		
L1	(compact same layout$1 same node$1 same edge$1) and (parent same descendent$1)	0	L1

END OF SEARCH HISTORY

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Search Results -

Terms	Documents
L8 and L14	0

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DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=ADJ			
L1	(compact$4 same node$1 same tree$1) and layout$1	101	L1
L2	(compact$4 same node$1 same tree$1) and layout$1 and (square with layout$1)	4	L2
L3	(node$1 same tree$1) and layout$1 and (square with bounding box$2)	76	L3
L4	network$3 same compact$4 same node$1	1328	L4
L5	L4 and (flow with diagram$1)	397	L5
L6	715/514.ccls.	455	L6
L7	715/734.ccls.	276	L7
L8	715/851.ccls.	93	L8
L9	L6 and L5	0	L9
L10	L6 and L4	0	L10
L11	L7 and L4	0	L11
L12	L7 and L5	0	L12
L13	L8 and L4	0	L13
L14	(compact$4 same node$1) and layout$1	885	L14
L15	L6 and L14	8	L15
L16	L7 and L14	0	L16
L17	L8 and L14	0	L17

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Search Results - Record(s) 1 through 14 of 14 returned.

1. Document ID: US 20050060672 A1

L2: Entry 1 of 14 File: PGPB Mar 17, 2005

PGPUB-DOCUMENT-NUMBER: 20050060672
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20050060672 A1

TITLE: Automated layout transformation system and method

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw Desc | Image

2. Document ID: US 20020075290 A1

L2: Entry 2 of 14 File: PGPB Jun 20, 2002

PGPUB-DOCUMENT-NUMBER: 20020075290
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20020075290 A1

TITLE: Incremental and interruptible layout of visual modeling elements

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw Desc | Image

3. Document ID: US 7134102 B2

L2: Entry 3 of 14 File: USPT Nov 7, 2006

US-PAT-NO: 7134102
DOCUMENT-IDENTIFIER: US 7134102 B2
** See image for Certificate of Correction **

TITLE: Automated layout transformation system and method

PRIOR-PUBLICATION:

DOC-ID	DATE
US 20050060672 A1	March 17, 2005

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

4. Document ID: US 6333656 B1

L2: Entry 4 of 14 File: USPT Dec 25, 2001

US-PAT-NO: 6333656
DOCUMENT-IDENTIFIER: US 6333656 B1

TITLE: Flip-flops

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw Desc | Image

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☐ 5. Document ID: US 6297668 B1

L2: Entry 5 of 14 File: USPT Oct 2, 2001

US-PAT-NO: 6297668
DOCUMENT-IDENTIFIER: US 6297668 B1

TITLE: Serial device compaction for improving integrated circuit layouts

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw Desc | Image

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☐ 6. Document ID: US 6256220 B1

L2: Entry 6 of 14 File: USPT Jul 3, 2001

US-PAT-NO: 6256220
DOCUMENT-IDENTIFIER: US 6256220 B1

TITLE: Ferroelectric memory with shunted isolated nodes

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw Desc | Image

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☐ 7. Document ID: US 6252448 B1

L2: Entry 7 of 14 File: USPT Jun 26, 2001

US-PAT-NO: 6252448
DOCUMENT-IDENTIFIER: US 6252448 B1

TITLE: Coincident complementary clock generator for logic circuits

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw Desc | Image

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☐ 8. Document ID: US 6198324 B1

L2: Entry 8 of 14 File: USPT Mar 6, 2001

US-PAT-NO: 6198324
DOCUMENT-IDENTIFIER: US 6198324 B1

TITLE: Flip flops

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw Desc | Image

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9. Document ID: US 5959878 A

L2: Entry 9 of 14 File: USPT Sep 28, 1999

US-PAT-NO: 5959878
DOCUMENT-IDENTIFIER: US 5959878 A

TITLE: Ferroelectric memory cell with shunted ferroelectric capacitor and method of making same

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw Desc | Image

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10. Document ID: US 4602270 A

L2: Entry 10 of 14 File: USPT Jul 22, 1986

US-PAT-NO: 4602270
DOCUMENT-IDENTIFIER: US 4602270 A

TITLE: Gate array with reduced isolation

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw Desc | Image

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11. Document ID: NB9008171

L2: Entry 11 of 14 File: TDBD Aug 1, 1990

TDB-ACC-NO: NB9008171

DISCLOSURE TITLE: Compact Dummy Word Line for Sense System Timing Chain.

PUBLICATION-DATA:
IBM Technical Disclosure Bulletin, August 1990, US

VOLUME NUMBER: 33
ISSUE NUMBER: 3B
PAGE NUMBER: 171 - 173

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw Desc | Clip Img

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12. Document ID: NN84102880

L2: Entry 12 of 14 File: TDBD Oct 1, 1984

TDB-ACC-NO: NN84102880

DISCLOSURE TITLE: Algorithm to Compact a VLSI Symbolic Layout With Mixed Constraints

PUBLICATION-DATA:
IBM Technical Disclosure Bulletin, October 1984, US

VOLUME NUMBER: 27
ISSUE NUMBER: 5
PAGE NUMBER: 2880 - 2887

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw Desc | Clip Img

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☐ 13. Document ID: NN71043262

L2: Entry 13 of 14 File: TDBD Apr 1, 1971

TDB-ACC-NO: NN71043262

DISCLOSURE TITLE: Method for Dynamic Storage Management. April 1971.

PUBLICATION-DATA:
IBM Technical Disclosure Bulletin, April 1971, US

VOLUME NUMBER: 13
ISSUE NUMBER: 11
PAGE NUMBER: 3262 - 3264

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw Desc | Clip Img

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☐ 14. Document ID: JP 06203104 A

L2: Entry 14 of 14 File: DWPI Jul 22, 1994

DERWENT-ACC-NO: 1994-282101
DERWENT-WEEK: 199435

TITLE: Layout compaction method of analog LSI circuit - involves cutting down of invalid domains by observation from node existing in predetermined position

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw Desc | Clip Img | Image

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Terms	Documents
compact$3 same node$1 same diagram$1 same layout$1	14

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Previous Page Next Page Go to Doc#

Terms used: **compacting node layouts** Found **16,802** of **216,199**

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1 Force-transfer: a new approach to removing overlapping nodes in graph layout
Xiaodi Huang, Wei Lai
February 2003 **Proceedings of the 26th Australasian computer science conference - Volume 16 ACSC '03**
Publisher: Australian Computer Society, Inc.
Full text available: pdf(311.27 KB) Additional Information: full citation, abstract, references, citings, index terms

Graphs where each node includes an amount of text are often used in applications. A typical example of such graphs is UML diagrams used in CASE tools. To make text information in each node readable in displaying such graphs, it is required there should be no overlapping nodes. This paper proposes the Force-Transfer algorithm to give a new efficient approach to removing overlapping nodes. The proposed approach employs a heuristic method to approximate the global optimal adjustment with the local ...

Keywords: force transfer, graph layout, mental map, neighbor nodes, node overlapping

2 An algorithm to compact a VLSI symbolic layout with mixed constraints
Y. Z. Liao, C. K. Wong
June 1983 **Proceedings of the 20th conference on Design automation DAC '83**
Publisher: IEEE Press
Full text available: pdf(462.46 KB) Additional Information: full citation, abstract, references, citings, index terms

A popular algorithm to compact a VLSI symbolic layout is to use a graph algorithm similar to finding the 'longest-path' in a network. The algorithm assumes that the spacing constraints on the mask elements are of the lower-bound type. However, to enable the user to have close control over the compaction result, a desired symbolic layout system should allow the user to add either the equality or the upper-bound constraints on selected pairs of mask elements as well. This paper proposes an al ...

3 Flexible layering in hierarchical drawings with nodes of arbitrary size
Carsten Friedrich, Falk Schreiber
January 2004 **Proceedings of the 27th Australasian conference on Computer science - Volume 26 ACSC '04**
Publisher: Australian Computer Society, Inc.
Full text available: pdf(383.34 KB) Additional Information: full citation, abstract, references, citings, index terms

Graph drawing is an important area of information visualization which concerns itself with the visualization of relational data structures. Relational data like networks, hierarchies, or database schemas can be modelled by graphs and represented visually using graph

drawing algorithms. Most existing graph drawing algorithms do not consider the size of nodes when creating a drawing. In most real world applications, however, nodes contain information which has to be displayed and nodes thus need a ...

Keywords: graph drawing, graph visualization, layering

4 An efficient compactor for 45° layout

David Marple, Michiel Smulders, Henk Hegen

June 1988 **Proceedings of the 25th ACM/IEEE conference on Design automation DAC '88**

Publisher: IEEE Computer Society Press

Full text available: pdf(1.28 MB) Additional Information: full citation, abstract, references, citings, index terms

This paper describes a one-dimensional compactor which works efficiently on basic VLSI layout. The compactor operates on a tiled layout structure which represents any VLSI layout containing 45° multiple angles. The compaction program performs both pitch minimization and wire length minimization in either X or Y directions. The compactor works quickly and efficiently due to the clever use of the layout structure and graph based Simplex method. The compactor corrects design rule violation ...

5 Compaction with incremental over-constraint resolution

W. L. Schiele

June 1988 **Proceedings of the 25th ACM/IEEE conference on Design automation DAC '88**

Publisher: IEEE Computer Society Press

Full text available: pdf(538.57 KB) Additional Information: full citation, abstract, references, citings, index terms

The occurrence and resolution of over-constraints in one-dimensional layout compaction will be discussed. A new algorithm is given which solves the longest path problem in the constraint graph and resolves all positive cycles either by constraint relaxation or by jog generation. The presented algorithm eliminates the positive cycles one at a time and reuses the intermediate results, which had been obtained up to the point when the cycle was detected. Thus, the amount of additional effort re ...

6 An efficient two-dimensional layout compaction algorithm

H. Shin, C.-Y. Lo

June 1989 **Proceedings of the 26th ACM/IEEE conference on Design automation DAC '89**

Publisher: ACM Press

Full text available: pdf(703.43 KB) Additional Information: full citation, abstract, references, citings, index terms

A new heuristic two-dimensional symbolic layout-compaction approach is developed. After conventional one-dimensional compaction steps, all the components on the critical paths that define the height or width of the given layout are found and rearranged to reduce the layout size. During this process, constraints in both x and y directions are considered and pitch-matching of ports for hierarchical compaction can be achieved to reduce the amount of the design ...

7 Technology tracking of non manhattan VLSI layout

J. Waterkamp, R. Wicke, R. Brück, M. Reinhardt, G. Schrammeck

June 1989 **Proceedings of the 26th ACM/IEEE conference on Design automation DAC '89**

Publisher: ACM Press

Full text available: pdf(614.75 KB) Additional Information: full citation, abstract, references, citings, index terms

Improvements in IC technologies make existing layout libraries obsolete. In order to reuse these layouts, adaptation to the requirements of new technologies have to take

place. In this paper a system is presented that automatizes this task using a locally two dimensional compaction algorithm. The system is able to handle arbitrary geometries and arbitrary technologies (including bipolar and mixed ones).

8 Power and area optimization by reorganizing CMOS complex gate circuits

M. Tachibana, S. Kurosawa, R. Nojima, N. Kojima, M. Yamada, T. Mitsuhashi, N. Goto

April 1995 **Proceedings of the 1995 international symposium on Low power design ISLPED '95**

Publisher: ACM Press

Full text available: pdf(77.57 KB) Additional Information: full citation, references, index terms

9 Compact layout of layered trees

Kim Marriott, Peter Sbarski

January 2007 **Proceedings of the thirtieth Australasian conference on Computer science - Volume 62 ACSC '07**

Publisher: Australian Computer Society, Inc.

Full text available: pdf(727.96 KB) Additional Information: full citation, abstract, references

The standard layered drawing convention for trees in which the vertical placement of a node is given by its level in the tree and each node is centered between its children can lead to drawings which are quite wide. We present two new drawing conventions which reduce the layout width to be less than some maximum width while still maintaining the essential layered drawing convention. These conventions relax the requirement that a parent must be exactly placed midway between its children, and i ...

10 A subjective review of compaction (tutorial session)

Y. Eric Cho

June 1985 **Proceedings of the 22nd ACM/IEEE conference on Design automation DAC '85**

Publisher: ACM Press

Full text available: pdf(932.88 KB) Additional Information: full citation, abstract, references, citings, index terms

Compaction is the CAD tool used to pack rough sketches or symbolic diagrams to produce IC layouts. Manual compaction is tedious, time-consuming, and error-prone; automated compaction tools can greatly shorten the layout design cycle. This paper reviews the historical background and the major developments in the field of compaction, emphasizing subjective evaluations rather than objective descriptions. The major approaches covered are constraint-graph, shear-line, and virtual-grid. Various i ...

11 A framework of filtering, clustering and dynamic layout graphs for visualization

Xiaodi Huang, Peter Eades, Wei Lai

January 2005 **Proceedings of the Twenty-eighth Australasian conference on Computer Science - Volume 38 ACSC '05**

Publisher: Australian Computer Society, Inc.

Full text available: pdf(304.40 KB) Additional Information: full citation, abstract, references, index terms

Many classical graph visualization algorithms have already been developed over the past decades. However, these algorithms face difficulties in practice, such as the overlapping node problem, large graph layout and dynamic graph layout. In order to solve these problems, this paper aims to systematically address algorithmic issues related to a novel framework that describes the process of graph visualization applications. First of all, a framework for graph visualization is described. As the impo ...

Keywords: clustering, filtering, framework, graph drawing, graph visualization, information visualization

12 Automatic data layout for distributed-memory machines

Ken Kennedy, Ulrich Kremer
July 1998 **ACM Transactions on Programming Languages and Systems (TOPLAS)**, Volume 20 Issue 4
Publisher: ACM Press

Full text available: pdf(633.20 KB) Additional Information: full citation, abstract, references, citings, index terms, review

The goal of languages like Fortran D or High Performance Fortran (HPF) is to provide a simple yet efficient machine-independent parallel programming model. After the algorithm selection, the data layout choice is the key intellectual challenge in writing an efficient program in such languages. The performance of a data layout depends on the target compilation system, the target machine, the problem size, and the number of available processors. This makes the choice of a good layout extremel ...

Keywords: high performance Fortran

13 Using spring algorithms to remove node overlapping

Wanchun Li, Peter Eades, Nikola Nikolov
January 2005 **proceedings of the 2005 Asia-Pacific symposium on Information visualisation - Volume 45 APVis '05**
Publisher: Australian Computer Society, Inc.
Full text available: pdf(464.59 KB) Additional Information: full citation, abstract, references, index terms

Cluttered drawings of graphs cannot effectively convey the information of graphs. Two issues might cause node overlapping when one draws a picture of a graph. The first issue occurs when applying a layout algorithm for an abstract graph to a practical application in which nodes are labeled. The second is the changing of a node's size in a dynamic drawing system. This paper presents two algorithms, *DNLS* and *ODNLS*, for removing the two kinds of overlapping. The algorithms are based o ...

Keywords: graph drawing, node overlapping, spring algorithm

14 Technology driven layout methodologies: Technology migration techniques for simplified layouts with restrictive design rules

Xiaoping Tang, Xin Yuan
November 2006 **Proceedings of the 2006 IEEE/ACM international conference on Computer-aided design ICCAD '06**
Publisher: ACM Press
Full text available: pdf(199.61 KB) Additional Information: full citation, abstract, references, index terms

Designs using simple geometric layout objects (such as points, sticks and rectangles) with Restrictive Design Rules (RDRs) on each layout object (i.e., it must be placed on a set of grids subject to a set of ground rules) have been introduced as an approach to better enable design for manufacturability (DFM) in ultra-deep submicron designs[9]. In this paper, we study the problem of migrating the conventional shape-based layouts to the simplified layouts with RDR constraints. We present a migr ...

15 Layout compaction with attractive and repulsive constraints

Akira Onozawa
January 1991 **Proceedings of the 27th ACM/IEEE conference on Design automation DAC '90**
Publisher: ACM Press

Full text available: pdf(777.87 KB) Additional Information: full citation, abstract, references, citings, index terms

A one-dimensional compaction algorithm with attractive and repulsive constraints is proposed. Depending on these constraints, the proposed algorithm shrinks[expands] the spaces among the specified layout elements without causing any design rule violations, as if some force were affecting them. It implies that the resultant layout has less cross talk and delay. The proposed network simplex algorithm experimentally proves to be efficient

in both time and space.

16 New graph bipartizations for double-exposure, bright field alternating phase-shift mask layout

Andrew B. Kahng, Shailesh Vaya, Alexander Zelikovsky

January 2001 **Proceedings of the 2001 conference on Asia South Pacific design automation ASP-DAC '01**

Publisher: ACM Press

Full text available: pdf(137.08 KB) Additional Information: full citation, abstract, references, citings, index terms

We describe new graph bipartization algorithms for lay-out modification and phase assignment of bright-field alternating phase-shifting masks (AltPSM) [25]. The problem of layout modification for phase-assignability reduces to the problem of making a certain layout-derived graph bipartite (i.e., 2-colorable). Previous work [3] solves bipartization optimally for the dark field alternating PSMregime. Only one degree of freedom is allowed (and relevant) for such a bipartization: edge deletion, ...

17 Improved compaction by minimized length of wires

W. L. Schiele

June 1983 **Proceedings of the 20th conference on Design automation DAC '83**

Publisher: IEEE Press

Full text available: pdf(444.79 KB) Additional Information: full citation, abstract, references, citings, index terms

The compaction of IC or hybrid layouts by means of the "longest path" method yields a slack in the placement of part of the elements, which, in its turn, can be used to reduce the overall wire-length. The result is an improved electrical performance and a smaller layout. The optimization problem was transformed to a graphtheoretical problem in a way similar to the compaction problem itself. Our procedure starts by adding pieces of information out of the connectivity of the layou ...

18 Dual quadtree representation for VLSI designs

S. K. Nandy, L. V. Ramakrishnan

July 1986 **Proceedings of the 23rd ACM/IEEE conference on Design automation DAC '86**

Publisher: IEEE Press

Full text available: pdf(532.30 KB) Additional Information: full citation, abstract, references, index terms

The Quad-CIF tree has been proposed as a data structure for hierarchical design of VLSI. Frequently encountered operations in VLSI design require a lot of search effort on a Quad-CIF tree. Additionally, since the empty spaces are not explicitly stored in the tree, layout compaction is difficult to achieve. To support such operations efficiently, we propose a dual quadtree structure for VLSI design. At the first level we represent a cell in the layout as a "painted quadtree". The ...

19 VLSI layout and packaging of butterfly networks

Chi-Hsiang Yeh, Behrooz Parhami, E. A. Varvarigos, H. Lee

July 2000 **Proceedings of the twelfth annual ACM symposium on Parallel algorithms and architectures SPAA '00**

Publisher: ACM Press

Full text available: pdf(358.87 KB) Additional Information: full citation, abstract, references, citings, index terms

We present a scheme for optimal VLSI layout and packaging of butterfly networks under the Thompson model, the multilayer grid model, and the hierarchical layout model. We show that when L layers of wires are available, an N-node butterfly network can be laid out with area 4N2/L2 log22 N + o (N

20 Poster abstracts: Evolutionary layout: preserving the mental map during the development of class models

Susanne Jucknath-John, Dennis Graf, Gabriele Taentzer
September 2006 **Proceedings of the 2006 ACM symposium on Software visualization SoftVis '06**
Publisher: ACM Press
Full text available: pdf(2.09 MB) Additional Information: full citation, abstract, references, index terms

It is vital for any developer to keep track of changes during his project. Thus, it is common practice to take static snapshots of single class diagrams. But to preserve the mental map, the layout of a class diagrams sequence is necessary.Therefore, we present in this paper requirements to layout a sequence of class diagrams and an approach for a layout algorithm to fulfill them. Our main idea was to see a sequence of class diagrams as the evolution of one graph over time. We expressed the graph ...

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